CLAIMS

What is claimed is:

1. A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins;

(b) storing primitives in each screen bin containing a portion of the primitive;

(c) rendering the screen bins, by row from top to bottom, into the pixel frame buffer;

(d) displaying at least one rendered screen bin before the rendering of all the screen bins has completed for the single pixel frame buffer.

2. A method as in claim 1, wherein step (d) further comprises the step of initiating the displaying of the screen bins rendered when the rendering is at least ½ completed.

3. A method as in claim 1, wherein step (d) further comprises the step of initiating the displaying of the screen bins rendered after at least one row of screen bins has completed rendering.

4. A method as in claim 1, further comprising the step of using a hardware interlock to ensure that the rendering step does not advance ahead of the display step.

5. A method as in claim 4, further comprising the step of using a row based hardware interlock to ensure that the rendering step does not advance ahead of the display step.

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6. A method as in claim 1, further comprising the step of executing the rendering and displaying steps concurrently within the same frame buffer.

7. A method as in claim 1, wherein step (d) further comprises using an independent timer to control toggling of the geometry buffer.

8. A method as in claim 1, further comprising the step of utilizing a double buffered pixel frame memory, wherein an input side and output side of the double buffered pixel frame memory toggle independently.

9. A method as in claim 8, further comprising the step of utilizing a double buffered frame memory, wherein the input side and output side of the double buffered frame memory toggle independently and the rendering step is at least one half of a field ahead of the display step.

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10. A method for enabling a single pixel frame buffer for simultaneous rendering and display in a computer image generator, comprising the steps of:

(a) dividing a geometry buffer into a plurality of screen bins;

(b) storing primitives in each screen bin the primitives touch;

(c) rendering the screen bins by row from top to bottom, into the pixel frame buffer;

(d) displaying at least one row of screen bins rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins takes place after a selected portion of the screen bins for a current field have been rendered.

11. A method as in claim 10 further comprising the step of reducing the transport delay without allowing the display step to overlap a rendering envelope.

12. A method as in claim 10 further comprising the step of reducing the transport delay and allowing the display step to overlap a rendering envelope.

13. A method as in claim 10 further comprising the step of rendering at least one row of screen bins before the display step begins.

14. A method as in claim 10 further comprising the step of reducing the transport delay by allowing the display step to overlap a rendering envelope without allowing pixels from a previous field to be displayed.

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Docket No. T9180 Revision-10/19/00

15. An image generator with a single pixel frame buffer enabled for simultaneous rendering and display, comprising:

(a) a geometry buffer divided into a plurality of screen bins;

(b) a plurality of primitives, stored in all of the screen bins that touch a screen region defined by the screen bin;

(c) a rendering engine, configured to render the primitives in the screen bins by row and from top to bottom;

(d) a display processor, configured to display at least one rendered screen bin on a display screen before the rendering engine has completed rendering all the screen bins.

16. An image generator as in claim 15, wherein the display processor begins to display the screen bins rendered when the rendering of the screen bins is ½ complete.

17. An image generator as in claim 15, wherein the display processor begins to display the screen bins rendered after at least one row of screen bins has completed rendering.

18. An image generator as in claim 15, further comprising a geometry engine configured to transform the database and the primitives used by the image generator.

19. An image generator as in claim 15, further comprising a real-time controller configured to receive real-time control information and compute the transformation matrices.

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20. A method for reducing the transport delay in a computer image generator, comprising the steps of:

(a) dividing a display screen into a plurality of screen bins which store every primitive that touches a screen region defined by the screen bin;

(b) rendering the primitives in the screen bins by row from top to bottom in a frame buffer;

(c) displaying at least one screen bin rendered into the frame buffer before the rendering of all the screen bins has completed.

21. A method as in claim 20 wherein step (c) further comprises the step of displaying the screen bins rendered when the rendering of the screen bins is ½ complete.

22. A method as in claim 20 wherein step (c) further comprises the step of initiating the display of the screen bins rendered after at least one row of screen bins has completed rendering.

23. A method as in claim 20 wherein step (c) further comprises the step of displaying the screen bins rendered before the rendering of all the screen bins has completed and restricting the rendering step from advancing past the display step.

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